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BIELE-007

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00726

Term-End Examination

June, 2015

BIELE-007 : NANO-ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. (a) What are the various interconnect issues for nano-scale MOSFET technology ? 5

(b) Explain 'hot-electron effect', in sub-micron technology. 5

2. (a) What is nano-lithography ? Discuss the difficulties associated with practical implementation of nano-lithography. 5

(b) Explain the phenomenon of velocity saturation in MOSFETs. 5

3. (a) What are the various scaling issues in nano-technology MOSFETs ? 5

(b) How is silicon-on-insulator technology different from silicon-on-nothing technology ? 5

4. Draw and explain the structure of FinFET. Discuss the similarities and dissimilarities in FinFET and multi-gate MOSFET. *10*

5. Write short notes on any ***two*** of the following : *2×5=10*

   (a) Coulomb-Staircase

   (b) Vertical MOSFETs

   (c) Multiple gate MOSFETs

6. (a) What do you understand by quantum well, quantum wire and quantum dot ? Give an example of each. *5*

   (b) What are the distinctive features of resonant tunneling in diodes ? *5*

7. Draw and explain the heterostructures of III-V and II-VI compounds with their energy band diagrams. *10*

8. (a) Explain the working of single electron devices with necessary diagrams. *5*

   (b) What are the different applications of resonant-tunneling devices ? What are the advantages of RTDs ? *5*

9. Explain Carbon Nano-tube Field Effect Transistor (CNFET). Derive the expression for theoretical value of drain current for CNFET. *10*

10. (a) What are the main features of SpinFET ? Draw and explain the I-V characteristics of SpinFET. *5*

(b) Explain the various steps of fabrication for SpinFET. *5*
