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BIEL-025

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00626

June, 2015

BIEL-025 : ADVANCED MICROPROCESSOR ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

1. Explain how instruction set, compiler technology, CPU implementation and control, cache and memory hierarchy affect the CPU performance and justify its effects in terms of program length, clock rate and effective cycles per instruction (CPI). *10*

2. Why do most RISC integer units use 32 general purpose registers ? Explain the relationship between the integer unit and the floating-point unit in most RISC processors using either scalar or superscalar organization. *3+7=10*

3. Explain and compare the following four cache memory organizations in terms of hardware complexity, implementation cost and flexibility in implementing "block replacement algorithm" :

$4 \times 2\frac{1}{2} = 10$

(a) Direct mapping cache

(b) Fully associative cache

(c) Set associative cache

(d) Sector mapping cache

4. A pipeline 'P' is found to provide a speed up of 6·16 when operating at 100 MHz and an efficiency of 88%.

(a) How many stages does 'P' have ?

(b) What are P's MIPS and CPI performance levels ? $5+5=10$

5. Define the following terms related to parallelism and dependence relation : $5 \times 2 = 10$

(a) Computational granularity

(b) Antidependence

(c) Bernstein conditions

(d) Degree of parallelism

(e) Communication latency

6. Compare the advantages and shortcomings in implementing private virtual memories and a globally shared virtual memory in a multicomputer system based on their latency, coherence, page migration and protection issues. *10*

7. Consider the following pipeline reservation table :

	1	2	3	4
S1	×			×
S2		×		
S3			×	

(a) What are the forbidden latencies ?

(b) Draw the state transition diagram.

(c) List all the simple and greedy cycles.

(d) Determine the optimal constant latency cycle and the minimal average latency.

(e) Determine the throughput of this pipeline with pipeline clock period $\tau = 20$ ns. *5×2=10*

8. (a) A magnitude-comparator circuit compares two unsigned numbers X and Y and produces three outputs Z_1, Z_2 and Z_3, which indicate X = Y, X > Y, and X < Y respectively. Show how to implement a magnitude comparator for 2-bit numbers using a single 16-input, 3-bit multiplexer of appropriate size. *10*

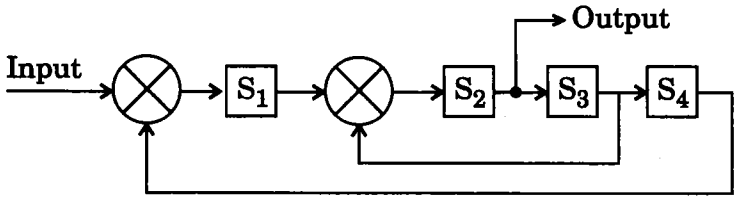
9. Discuss the impact of the following design decisions on cache performance : *3+3+4=10*

(a) Selection of a cache block (line) size p1, which is quite small.

(b) Selection of a cache block size, which is too big.

(c) Selection of an associativity level 'k' that is too small.

10. Consider the pipelined processor with a total evaluation time of six clock cycles. All successor stages must be used after each clock cycle. $4 \times 2\frac{1}{2} = 10$



(a) Specify the reservation table for this pipeline.

(b) List the set of forbidden latencies between task initiations.

(c) List all greedy cycles from the state diagram.

(d) What is the maximum throughput of this pipeline ?