No. of Printed Pages : 4

BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2015

00126

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Assume suitable missing data, if any. Use of scientific calculator is permitted.*

1. Explain the following terms of op-amp : $4 \times 2\frac{1}{2} = 10$

(a) CMRR

(b) Slew Rate

(c) PSRR

(d) Gain

2. Design a multiplier using squaring circuits. How is it different from multiplying quad approach ? *10*

3. (a) Which is the most basic DAC architecture ? Explain its basic operation principle.

(b) Design a 3-bit DAC using an R – 2R architecture with R = 1 kΩ, R_F = 2 kΩ and V_{REF} = 5 V. Assume that the resistances of the switches are negligible. Determine the value of i_{TOTAL} for each digital input and the corresponding output voltage, V_{out}. *2×5=10*

4. (a) Explain the pipeline architecture of ADC.

(b) Differentiate between single-slope ADC and dual-slope ADC. Explain them with block diagrams. *2×5=10*

5. Explain the operation principle of a two-stage op-amp. What is the need of compensation in op-amp ? How do you estimate the bandwidth in op-amp circuits ? *10*

6. Explain the operation principle of band-pass and high-pass sync filters. How is it different from interpolating filters ? *7+3=10*

7. (a) Draw the process flow of sub-micron CMOS technology for inverter circuits.

(b) How is MOS capacitor fabricated and characterized ? Explain with suitable process flow diagrams. *2×5=10*

8. (a) What are the short-channel effects in MOSFET ? How can these be avoided ?

(b) Draw the small-signal models of MOSFET considering channel length modulation and body effect by a dependent current source or/and by a resistor. *2×5=10*

9. (a) Consider the amplifier as shown in Figure 1, with $(W/L)_{1-4} = 50/0{\cdot}5$, $I_{SS} = 1$ mA, and input CM level of 1·3 V. Calculate the small-signal gain and the maximum output swing if all transistors remain in saturation.

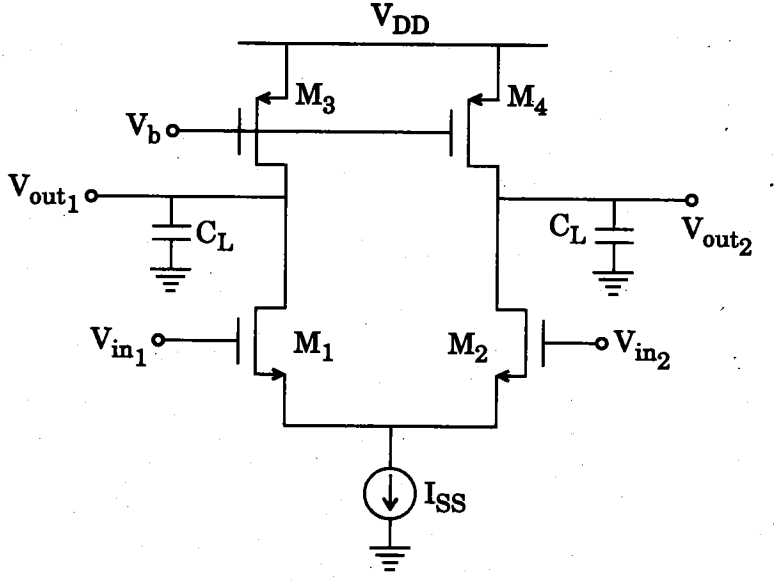

Figure 1

(b) Suppose all PMOS enters into the triode region by 50 mV, so as to increase the allowable differential swing by 100 mV. What is the small-signal gain at the peaks of the output swing ? *7+3=10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) S/H Characteristics

(b) Flash ADC

(c) Cyclic DAC