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BIEL-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00676

Term-End Examination

June, 2015

BIEL-003 : DIGITAL ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions in all. All questions carry equal marks.*

1. Minimize the following logic function using K–maps and realize using NAND and NOR gates : *10*

$F(A, B, C, D) = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$.

2. (a) Simplify the following expression using Boolean algebra technique : *5*

$$Z = AB + A(B + C) + B(B + C).$$

(b) Distinguish between minterms and maxterms. *3*

(c) What are Universal gates ? *2*

3. (a) Draw the logic diagram of a full subtractor using half subtractors and explain its working with the help of a truth table. *7*

(b) What is meant by priority encoder ? *3*

4. (a) Design a 32 : 1 multiplexer using two 16 : 1 multiplexers and a 2 : 1 multiplexer. 5

(b) Implement the following function using a 3-line to 8-line decoder : 5

$S(A, B, C) = \sum m(1, 2, 4, 7)$

$C(A, B, C) = \sum m(3, 5, 6, 7)$

5. (a) With the help of a suitable diagram, explain how you convert a JK flip-flop to a T type flip-flop. 5

(b) What is a flip-flop ? What is the difference between a latch and a flip-flop ? List out the application of flip-flop. 5

6. What are synchronous counters ? Design a Mod-5 synchronous counter using JK flip-flops. 10

7. Draw TTL circuit for Totem-pole output and explain its working. Why is it not used for WIRED AND connection ? 10

8. (a) What are the advantages of CMOS logic ? Explain CMOS Inverter with the help of a neat diagram. 6

(b) Discuss briefly the concept of PLA. 4

9. (a) Draw the logic diagram of 16-bit ROM Array and explain its principle of operation. 6

(b) The capacity of 2k × 16 PROM is to be expanded to 16k × 16. Find the number of PROM chips required and the number of address lines in the expanded memory. 4

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Digital Comparator

(b) Algorithmic State Machines

(c) Flash Memory