B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

June, 2015

00510

BICS-009 : LOGIC DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. (a) Implement the given Boolean function using NAND gates only : 5

$$F(x, y, z) = \Sigma(1, 2, 3, 4, 5, 7).$$

(b) Express the complement of

$F(A, B, C, D) = \Sigma(3, 5, 9, 11, 15)$ in sum of minterms form. 5

2. (a) Draw the diagram of digital circuit for the function 3

$F(a, b, c) = (A + B) \cdot (\overline{A} + \overline{C}) \cdot (B + C)$.

(b) Simplify the following Boolean function using QM method : 7

$F(A, B, C, D) = \Sigma(0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$.

3. Implement 3-bit odd parity generator using JK flip-flop, with the help of state diagram, state table, transition table and excitation table. *10*

4. (a) Add 5 and –7 and subtract 48 and –23 using 2's complement method. *5*

   (b) Implement Full adder using two half adders. *5*

5. (a) Define latch and flip-flop. Implement the D flip-flop using JK flip-flop. *5*

   (b) What is race around condition ? How can it be removed ? *5*

6. (a) Explain 4-bit parallel in serial out shift register with the help of a suitable diagram. *5*

   (b) Define modulus of counter. How can you change modulus of counter ? *5*

7. (a) List the specifications of A/D converter and explain dual-slope A/D converter using suitable diagram. *5*

   (b) Explain 3-bit R-2R ladder D/A converter. *5*

8. Draw the state diagram, state table and ASM chart for a sequence detector to detect the sequence 0110. *10*

   Note : Overlapping is permitted.

9. (a) Which TTL series is most suitable at high frequencies and which gates are suitable for the wired AND operation ? Justify your answer. *5*

(b) Compare CMOS with TTL. *5*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) 2 Input CMOS NOR GATE

(b) Decade Counter

(c) TTL to CMOS Interface