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BIELE-015

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00545

Term-End Examination

June, 2019

BIELE-015 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Any missing data may be suitably assumed.*

1. (a) How does processor communicate with the I/O devices with the help of interface circuit ? *5*

(b) Write down the classification of various instruction formats. *5*

2. (a) Explain the limitation and format of Fixed Point numbers and Floating Point numbers. *5*

(b) Give the circuit diagram of a 4-bit parallel in parallel out register and explain its working. *5*

3. (a) Give the flow chart for division of floating point number and explain. 5

(b) What is 2's complement representation ? Explain binary subtraction using 2's complement method. 5

4. (a) Explain step-by-step, using Booth's algorithm, the multiplication of (-5) with (-2). 5

(b) What are the advantages and disadvantages of hardwired control and software control systems ? 5

5. (a) Explain instruction level pipeline process. 5

(b) What are the similarities and differences between superscalar operation and parallel processing ? 5

6. (a) What is meant by 'mapping' ? 4

(b) In how many ways can mapping be implemented ? 3

(c) What is the role of cache directory in mapping ? 3

7. Explain the concept and structure of associative memory in detail with the help of neatly labelled block diagram. 10

8. (a) A block set associative cache consists of a table of 64 blocks divided into four blocks set. The main memory contains 4096 blocks, each consisting of 128 words.

(i) How many memory bits are there in a main memory address ?

(ii) How many bits are there in each of the tag, index and word bits ?

(iii) What is the size of cache memory ? *5*

(b) What is the difference between an isolated mapped I/O and a memory mapped I/O ? *5*

9. (a) Why is the address bus in DMA controllers bi-directional ? Is it possible to suddenly terminate the ongoing DMA operation before the completion of all data transfer ? *5*

(b) What are interrupts ? Explain various types of interrupts. *5*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Segmented Page Mapping

(b) Multilevel Memory System

(c) Fault Tolerance