No. of Printed Pages : 3

BIELE-011

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00525

Term-End Examination

June, 2019

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

1. (a) Simplify the 4-variable logic function using K-map

$$F(A, B, C, D) = \pi M(4, 6, 10, 12, 13, 15).$$ *5*

(b) Implement the following Boolean function with NOR gates only : *5*

$$F(A, B, C, D) = A(BC + D) + \bar{A}B$$

2. (a) Implement the full subtractor using 1 : 8 demux. *5*

(b) Write down the various applications of counters and shift registers. *5*

3. Design a synchronous, recycling MOD-8 binary down counter using D-Flip Flop. *10*

4. (a) Differentiate between synchronous and asynchronous circuits with appropriate examples. 5

(b) Draw the state diagram for BCD counter. 5

5. Draw and explain the architecture of system controller. 10

6. Explain various types of hazards in digital circuit. Implement a hazard free circuit realization for the following function : 10

$$F(A, B, C, D) = \bar{A}BC + \bar{A}\bar{B}C + B\bar{C} + \bar{A}C$$

7. (a) Realize the following 3 switching functions with a 3-input, 3-output PROM : 5

$$f_1(A, B, C) = AB + \bar{B}C$$

$$f_2(A, B, C) = (A + B + C)\ (\bar{A} + B)$$

$$f_3(A, B, C) = A + \bar{B}C$$

(b) Enlist the various applications of ROM, PROM and FPLA in system controller design. 5

8. (a) Draw and explain the block diagram of programmable system controller. 5

(b) Describe the application of MC2900 in system control design. 5

9. (a) Differentiate between behavioural, dataflow and structural models of VHDL. 5

(b) Write a VHDL code for J-K Flip Flop. 5

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Design of Asynchronous Machine

(b) MSI Decoder

(c) Data Objects in VHDL