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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00655

June, 2019

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. (a) What are the different levels of abstraction in VHDL ? Explain with suitable diagram. *5*

(b) Explain design flow for digital system design using VHDL. *5*

2. (a) Write a procedure for BCD to SSD conversion in VHDL for common anode type of seven segment display. *5*

(b) Write the VHDL code for basic functional unit of a dynamic shift register. *5*

3. What is FSM ? Explain the difference between Mealy and Moore machine with example. Write VHDL code for mod-7 counter using FSM. *10*

4. (a) Describe procedural continuous assignment statements assign, de-assign, force and release in VHDL. 5

(b) Write VHDL code for a traffic light controller. 5

5. (a) Define VLSI Testing. Explain different types of testing. 5

(b) Explain the different types of testing in test-pattern generation for BIST. 5

6. (a) What is the advantage of weighted pseudo random pattern generator over the normal method ? 5

(b) What is the advantage of pseudo exhaustive pattern generator over exhaustive pattern generator ? 5

7. (a) Explain the advantages of boundary scan description language. 5

(b) Write down the syntax for library and package declaration in VHDL. 5

8. (a) Give an example of a logic circuit in which stuck-at-0 and stuck-at-1 faults are indistinguishable. 5

(b) Differentiate between behavioural and structural modelling. Explain with suitable example. 5

9. (a) Explain different features of simulation semantics. *2*

(b) Differentiate between signal and variable in VHDL with suitable example. *3*

(c) Write a behavioural level VHDL code for 4×1 multiplexer circuit with appropriate circuit diagram. *5*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) FPGA

(b) Design Verification

(c) Adhoc DFT Method