No. of Printed Pages : 2

BIEL-025

00525

B.Tech. - VIEP - ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2019

BIEL-025 : ADVANCED MICROPROCESSOR ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *(i) Attempt **any seven** questions.*

*(ii) **All** questions carry **equal** marks.*

---

1. (a) What are the factors which affect the performance of a vector processor ? **5**

(b) How are multiple issue machines different from vectored machines ? Explain briefly. **5**

2. (a) Write and explain the instruction execution cycle followed by a typical processor. **5**

(b) What are the problems encountered in the implementation of pipelined processor ? **5**

3. (a) What do you mean by write assembly cache ? How is it useful ? **5**

(b) What are the design issues for multiprocessor systems ? Explain. **5**

4. What is pipelining ? Explain various hazards involved in implementing pipelining. **10**

5. (a) Explain the instruction level parallelism with dynamic approaches. 5

(b) Explain the models of memory consistency. 5

6. (a) Explain the categories of misses and how will you reduce cache miss rate. 7

(b) What is Dynamic Scheduling ? 3

7. Define multi-threading. Explain how ILP is achieved using multi-threading with an example. 3+7

8. Explain in detail, the architecture support for protecting processes from each other via virtual memory. 10

9. (a) With a neat diagram, explain the basic structure of a centralized share memory and distributed shared memory multiprocessor. 7

(b) What is static branch prediction ? 3

10. (a) Give a brief explanation about trends in power and costs in integrated circuits. 5

(b) What are the key issues in implementing advanced speculation techniques ? Explain in detail. 5