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BIEL-012

B.TECH. - VIEP - ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination, 2019

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : Three Hours] **[Maximum Marks : 70**

Note : Answer **any seven** questions. **All** questions carry **equal marks**. Missing data if any may be suitably assumed. Use of scientific calculator is permitted.

1. (a) How analog signals are converted into digital signals ? [2.5]

   (b) What are the issues of mixed signal layout design ? [2.5]

   (c) Define slew rate of OP Amp. [2.5]

   (d) Define CMRR (Common Mode Rejection Ratio) of Op Amp. [2.5]

2. (a) An analog signal in the range 0 to +10V is to be converted to 8 – bit digital signal. What is the resolution of the conversion in volts ? What is

the digital representation of an input of 6v ? What is the representation of an input of 6.2v ? What is the error made in the quantization of 6.2v in absolute terms and as a percentage of the input? What is the largest possible quantization error as a percentage of full scale ? [7]

(b) Explain the sampling process of analog signals and signal quantization. [3]

3. (a) Explain the working principle of DAC using R-2R ladder network. [5]

(b) If the input bias current of an OP-Amp, used as summer in a 10-bit DAC, is to be no more than ¼ LSB, what is the maximum current required to flow in for an OP-Amp whose bias current is as great as 0.5 μA ? [5]

4. (a) What are the types of ADC architectures available ? Explain pipeline architecture of ADC.[5]

(b) Consider the 5-bit charge redistribution converter with V_{REF} = 4V what is the voltage increment appearing on the top plate when S_5 is switched ? What is the full-scale voltage of this converter ?

If V_A -= 2.5V, which switches will be connected to V_{REF} at the end of conversion ? [5]

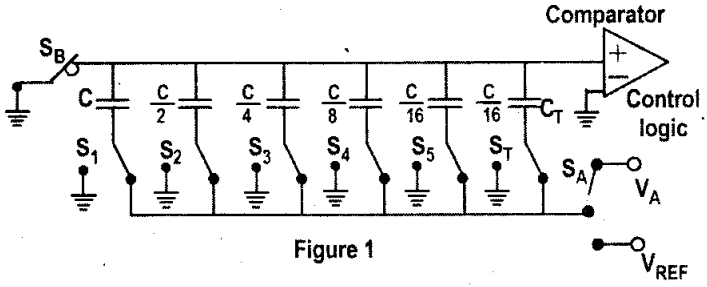

Figure 1

5. (a) Explain the static and dynamic characteristics of a comparator. [5]

(b) Draw the CMOS circuit of two stage comparator and explain its operation principle. Describe the frequency response of the two-stage, open-loop comparator. [5]

6. (a) Design a CMOS circuit for analog multiplier and explain its working principle. [5]

(b) Describe the use of level shifting circuits in analog circuit design. [5]

7. (a) Explain the use of SNR (Signal to Noise Ratio) in analog circuit design. How SNR is improved using averaging of signal ? [5]

(b) Differentiate between decimating filters for ADC and interpolating filters for DAC. [5]

8. (a) How sub-micron CMOS circuit design is different from conventional CMOS circuit design ? Explain. [5]

(b) Describe the process flow of sub-micron CMOS circuit design using suitable diagram. [5]

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