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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00063

June, 2018

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

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1. (a) Define different data objects and types used in VHDL. *5*

(b) What is architecture body ? Also give different modelling styles. *5*

2. Define inertial delay model and transport delay model with suitable examples. *10*

3. (a) Discuss FPGA architecture. *5*

(b) What is a look-up table used with FPGA design ? Illustrate with one example. *5*

4. Write a structural VHDL program corresponding to NAND gate based 2-input multiplexer. *10*

5. Write the operating principle and draw the system schematic of any ***two*** of the following : *5+5=10*

(a) Scan-path design method

(b) Scan-set design method

(c) Random-access scan

6. (a) Differentiate between stuck-at-faults and bridging faults. *5*

(b) For a 3-input NAND gate, prepare a table for detecting all possible stuck-at-faults. *5*

7. (a) Write a VHDL description of an S-R latch using process. *5*

(b) Draw the block diagram of a 4-bit magnitude comparator. *5*

8. (a) Briefly describe logical faults in digital devices. *5*

(b) Discuss controllability and observability regarding testing of digital circuits. *5*

9. Draw the architecture of Built-in-Self-Test (BIST) technique with suitable examples. *10*

10. Write short notes on any ***two*** of the following : *5×5=10*

(a) IEEE 1164 Standard

(b) VHDL Attributes

(c) Mealy and Moore Model