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BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

007703 **Term-End Examination**

June, 2018

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. Discuss various mixed-signal layout issues with appropriate examples. *10*

2. Define the following ADC specifications : *2×5=10*

(a) Quantization Levels

(b) Quantization Error

(c) Offset Error

(d) Gain Error

(e) Aliasing

3. Explain the following terms : *4+3+3=10*

   (a) Power supply and grounding issues

   (b) Shielding

   (c) Interconnect considerations

4. Explain the R-2R DAC architecture and derive an expression for its output voltage. *10*

5. Give the architecture of a 3-bit flash type ADC. Explain its operation with necessary mathematical expressions. *5+5=10*

6. What are analog multipliers ? Explain the operation of a 4-quadrant analog multiplier with the help of a neatly labelled circuit diagram and mathematical expressions. *2+4+4=10*

7. Explain how multiplier design can be obtained using squaring circuits. *10*

8. Explain the operation of interpolating filters for DAC to improve their SNR. *10*

9. Explain the process flow steps carried out in the Submicron CMOS design of Capacitors and Resistors. *10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Level shifting for analog multipliers

(b) Successive approximation ADC

(c) Characteristics of Sample and Hold (S/H) Circuit
