$\boxed{\textbf{BICS-025}}$

B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

00883

June, 2018

BICS-025 : ADVANCED COMPUTER ARCHITECTURE

Time : 3 hours   *Maximum Marks : 70*

Note : *Answer any **seven** questions. All questions carry equal marks.*

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1. (a) Draw a dataflow graph for the following sample program :   5

   input d, e, f

   $C_0 = 0$

   for i = 1 to 8 do

       begin

       $a_i = d_i + e_i$

       $b_i = a_i * f_i$

       $c_i = b_i + c_{i-1}$

       end

   output a, b, c

(b) How many cycles are required to execute through a sequential execution (i.e. Von Neumann machine) ? Illustrate. *5*

2. (a) Draw a four segment pipeline and its related space-time diagram to execute six tasks. Assume that in one clock cycle one task is executed. Also derive a speedup ratio for executing n tasks in a pipeline. *5*

(b) How are data dependency conflicts managed in an instruction pipeline ? Discuss. *5*

3. Define the following terms with respect to interconnection architecture with examples : *10*

   (a) Node degree
   (b) Static interconnection network
   (c) Network diameter
   (d) Multistage network

4. (a) What is the use of prefetch buffers in an instruction pipelining ? What are its types ? Describe its operations with the help of a diagram. *7*

(b) What are the two types of software parallelism ? Discuss. *3*

5. (a) Discuss control complexity, potential for parallelism and cost effectiveness of Von Neumann and dataflow machines. *6*

(b) Describe important parameters to measure performance of interconnection networks. *4*

6. **(a)** Draw a 3 × 3 mesh network and define its interior node degree and network diameter. Also comment on scalability and complexity of the network.   *5*

(b) Differentiate between static and dynamic interconnection network. List three networks in each category.   *5*

7. Explain matrix multiplication algorithm for SIMD architecture with the help of an example.   *10*

8. **(a)** Describe a system bus architecture for a multiprocessor system.   *5*

(b) Draw an 8 × 8 multistage switching network having three stages and four switches in each stage. Show all input and output lines.   *5*