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BICS-022

B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

00313 **Term-End Examination**

June, 2018

BICS-022 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. All questions carry equal marks.*

1. Differentiate between the following in the context of Instruction Set Architecture : *10*

(a) Register memory ISA vs Load store ISA

(b) Byte addressing vs Word addressing

(c) Variable length instruction format vs Fixed length instruction format

(d) Conditional branches vs Procedure calls

(e) Floating point single precision number vs Floating point double precision number

2. (a) Explain the concept of pipelining with the help of a diagram. What is the speedup that can be obtained by using pipelining ? *5*

(b) What are branch hazards in the context of instruction pipelining ? How does it affect the performance of pipelining ? Explain with the help of an example. *5*

3. (a) What is Amdahl's law ? How does this law define speedup ? *5*

(b) Consider the following assembly program segment : *5*

```
LOAD R1, A        ; Load content of memory location A to R1 register
LOAD R2, B        ; Load R2 with content of B
ADD R3, R2, R1    ; R3 ← R2 + R1
STOR C, R3        ; Store the result R3 into memory location C
```

Identify all the data dependencies in the code above. Which of the instructions in the above sequence can be executed in parallel ?

4. (a) What is dynamic scheduling in the context of instruction level parallelism ? Explain with the help of an example. Why is dynamic scheduling needed ? *5*

(b) What are multiple-issue processors ? Explain how the approach of multiple-issue of instruction is different in statically scheduled superscalar processors and VLIW processors. *5*

5. (a) What is branch target buffer ? How can it enhance the performance of a pipeline ? 5

(b) Explain the following terms in the context of instruction level parallelism : 5

(i) Thread level parallelism

(ii) Optimising compilers

6. (a) A computer requires to operate mostly using a vector instruction. Which of Flynn's category will be most applicable for such a computer ? Justify your answer. Also give example of a vector instruction. 5

(b) A cluster of computers can be classified under what category of Flynn's classification ? Justify your answer. Also explain the types of applications that can be solved by a cluster of computers. 5

7. Describe the structure of the following with the help of a diagram : 10

(i) Centralised shared memory multiprocessor

(ii) Distributed memory multiprocessor

Also give one disadvantage of each.

8. (a) Explain the directory-based cache coherence problem with the help of a diagram. 5

(b) Explain the relaxed consistency model in the context of multiprocessor systems. 5

9. Define the following with the help of formula (if needed) : *10*

(a) Set associative cache

(b) Direct mapped cache

(c) Miss rate of cache

(d) Miss penalty of cache

(e) Compulsory cache misses

(f) L1 cache

(g) L2 cache

(h) Average memory access time when cache is present

(i) Conflict of block placement in cache

(j) Hit time/hit rate of cache

10. Explain any ***four*** of the following with the help of a diagram/example, if needed : *10*

(a) Protection in virtual memory

(b) Cache coherence in multiprocessors

(c) SISD category of processors

(d) Control hazard in pipelining

(e) Return address predictors in the context of pipelining

(f) DRAM