No. of Printed Pages : 4

MCS-012

MCA (Revised) / BCA (Revised)
Term-End Examination
June, 2018

01205

MCS-012 : COMPUTER ORGANISATION AND ASSEMBLY LANGUAGE PROGRAMMING

Time : 3 hours *Maximum Marks : 100*

(Weightage 75%)

Note : *Question number **1** is **compulsory** and carries 40 marks. Attempt any **three** questions from the rest.*

1. (a) Convert the following pairs of decimal numbers to 8 bit signed 2's complement binary numbers and add them. State whether or not overflow occurs in each case. *6*

(i) 34 and 63

(ii) – 63 and – 24

(iii) – 86 and 19

(iv) – 34 and – 96

(b) Simplify the following Boolean expression in SOP form using the K-map : *5*

$F(A, B, C, D) = \Sigma(0, 1, 2, 8, 9, 10, 14, 15)$.

(c) Two 16 bit registers R0 and R1 contain binary values – 97 and + 76 respectively. Carry flag C = 1. What is the result of the following micro-operations : 6

(i) Add R0 and R1 with Carry

(ii) R0 AND with complement R1

(iii) Shift right R1 without carry

(iv) Selective set R1 using R0

(d) Explain the IEEE-32 bit format for single precision floating point representation. Represent

(i) $8{\cdot}75 \times 10^{6}$

(ii) $-0{\cdot}25 \times 10^{-5}$

using this format. 6

(e) How many chips of 512 K × 8 are required for constructing 4 M × 32 memory ? 3

(f) Write a program using 8086 assembly language program to find the larger of two byte values stored in memory location. Store the larger value in BL register. 6

(g) Discuss the data storage scheme used for hard disks. 4

(h) Discuss the indexed addressing scheme with the help of an example. 4

2. (a) Explain the process of error detection using even parity bit scheme. 4

(b) Explain the Hamming error correcting code for 4 bit data using an example. 6

(c) Explain the use of segment registers in 8086 microprocessors. Calculate the physical address given : 6

(i) IP = 2345h

(ii) CS = 1111h

(d) Explain the concept of memory interleaving. 4

3. (a) Explain the construction of J-K flip-flop with characteristic table and excitation table. 6

(b) Explain the construction of a full adder using half adders. 6

(c) Assume a computer has 32 word RAM having word size of 8 bits and cache memory of 4 blocks (block size = 16 bits). Where will be the main memory (RAM) address 12 located in cache if : 8

(i) Associative cache mapping scheme is followed ?

(ii) Direct cache mapping scheme is followed ?

4. (a) Explain how a pipelined processor results in better performance. *5*

(b) Explain the interrupt processing in 8086 with the help of a diagram. *5*

(c) Discuss any five features of RISC machines. *5*

(d) Differentiate between hardwired and microprogrammed control units. *5*

5. (a) Write a 8086 assembly language program to interchange two byte sized numbers stored in consecutive memory locations. *5*

(b) Explain the following with the help of an example, if needed : *15*

(i) Interrupt cycle

(ii) Program controlled I/O

(iii) Flash memory

(iv) 8086 flags

(v) NEAR procedure in 8086 microprocessor