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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00884

June, 2017

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. Draw the VHDL model of any digital system and explain each block in detail. *10*

2. (a) Write the VHDL code for Full Adder using Boolean expression. *5*

(b) Define Data objects and Identifiers with suitable examples. *5*

3. (a) Write the VHDL structural model for the circuit shown in Figure 1. 5

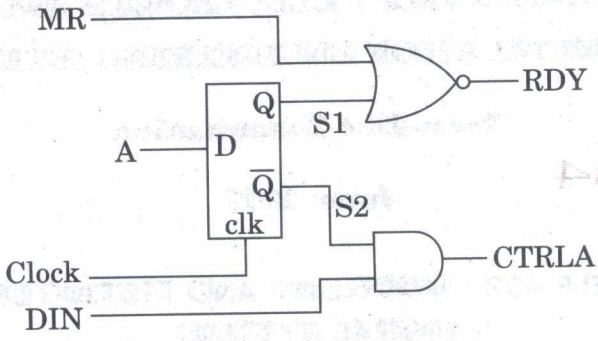

Figure 1

(b) Explain configurations. Why are they needed ? 5

4. Describe the structural model for the half and full subtractor circuit. 10

5. Differentiate between functional and structural fault models with suitable examples. 10

6. (a) What are delay fault models ? Explain their types. 5

(b) Draw the circuit of NAND and NOR gate using delay fault model. 5

7. (a) Explain the relationship among various fault models with suitable diagram. *5*

(b) Derive a minimal test set for the 4-bit Ripple-Carry Adder using single cell fault model. *5*

8. (a) Derive a three-valued truth table for a gate whose two-value logic behaviour is described by the following truth table : *5*

$v(C_{i1})$ \ $v(C_{i2})$	0	1
0	1	0
1	1	1

(b) What is a subprogram ? Explain it with a suitable example. *5*

9. (a) Write a short note on different types of faults found in digital circuits. *5*

(b) Design a 3-bit modulo-8 asynchronous counter using master-slave D-flip-flop. *5*

10. (a) Discuss built-in self-test for digital circuit. *5*

(b) Design a reconfigurable register that can be configured in the normal and test pattern generator modes. *5*