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BIELE-002

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00014

June, 2017

BIELE-002 : MICROELECTRONICS TECHNOLOGY

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. Assume suitable missing data, if any. Use of scientific calculator is permitted.*

1. Explain different lithographic techniques used in the microelectronics industry. *10*

2. With a neat labelled diagram, describe the steps and set-up of ion implantation in detail. *10*

3. With the help of a diagram, explain the fabrication steps for a silicon gate NMOS transistor. *10*

4. (a) What is Etching ? Explain RIE technique. *5*

   (b) Differentiate between dry etching and wet etching processes. *5*

5. Explain the steps involved in the CMOS process flow for multilevel metal formation. *10*

6. What are the factors to be considered for proper crystal growth from the melt ? *10*

7. (a) What is Epitaxy ? What are the characteristics of epitaxial growth ? *5*

   (b) Explain the molecular beam epitaxy method by drawing its schematic diagram. *5*

8. (a) Explain the properties of thermal oxides of silicon. *5*

   (b) Explain Electro-migration. *5*

9. Explain the following crystal structures with diagram and their characteristics with examples : *10*

   (a) Diamond Cubic Structure

   (b) Face-Centred Cubic Structure

10. Write short notes on any ***two*** of the following : *2×5=10*

    (a) Local Oxidation

    (b) Annealing Characteristics of Silicon

    (c) Sheet Resistance
