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BIEL-012

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00664

Term-End Examination

June, 2017

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Missing data, if any, may be suitably assumed. Use of scientific calculator is permitted.*

1. (a) Briefly explain the ADC specifications. 5

(b) Discuss the issues involved in mixed signal circuit layout. 5

2. (a) Describe the pipelined ADC with a neat diagram. 5

(b) For an 8-bit pipelined ADC, all the amplifiers had a gain of 2·1 instead of 2. If V_{in} = 3 V and V_{ref} = 5 V, what would be the resulting digital output, assuming other components are ideal ? 5

3. Draw the CMOS analog multiplier and explain its working. *10*

4. Develop an expression for effective number of bits in terms of the measured SNR, if the input wave has a peak amplitude of 30% of V_{ref}. *10*

5. With the help of neat relevant diagrams, describe the CMOS process flow for devices with $L_{min} < 0{\cdot}35\ \mu m$. *10*

6. (a) Describe the working of an R-2R ladder network with a neat diagram. *5*

   (b) Explain the working of a bandpass filter with neat circuit diagram. *5*

7. (a) Draw the 4-bit pipelined adder and describe how does it operate. *5*

   (b) Draw the positive edge-triggered delay using clocked CMOS logic. *5*

8. Explain how MOSFET behaves as a capacitor. Also explain floating MOS capacitor. *10*

9. (a) Determine the ideal SNR of an 8-bit data converter with an average of 20 outputs. *5*

(b) Bring out the principle of interpolation. *5*

10. (a) Write down the ideal characteristics of an op-amp. *5*

(b) What is current steering and how is it implemented ? *5*

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