No. of Printed Pages: 3 BIEL-003

Maximum Marks: 70

B.Tech. - VIEP - ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2017



Time: 3 hours

BIEL-003 : DIGITAL ELECTRONICS

Note: Attempt any seven questions. All questions carry equal marks. Assume any missing data suitably. Use of scientific calculator is allowed.

- Perform $(54)_{10} (27)_{10}$ using 2's complement. 5
 - Convert the following expressions into their canonical forms:
 - F = AB + ACD + ABC(i)
 - F = (A + B) (A + C) (B)(ii)
- 2. (a) Design and implement a 3-bit magnitude comparator. bus square and surface (d) 5
 - Design a 4-bit parallel adder. (b)

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BIEL-003

P.T.O.

3.	(a)	What do you mean by Master-Slave	
		flip-flop ? How does it avoid the race around condition ?	5
	(b)	What do you mean by characteristic	
		equation of flip-flop ? Derive it for	
		JK flip-flop.	5
4.	(a)	Differentiate between asynchronous and	!!
		synchronous counter.	5
	(b)	Design a 3-bit bidirectional synchronous	
		counter using T-flip-flop.	5
		diamental and the second	VPIII
5.	What	t do you mean by tri-state logic? Draw and	
	expla	in the working of a tri-state TTL NAND	
	gate.	그러워 다른 성하다면 이번 하는 경험을 많은 그게 가지가 그리고 있습니다.	10
	0		
6.	(a)	Design and implement 64k × 8 RAM using	
6.	(a)	Design and implement $64k \times 8$ RAM using $8k \times 8$ RAM.	5
6.		$8k \times 8$ RAM.	5
6.	(a) (b)	$8k\times 8$ RAM. Explain how a CMOS logic IC can be driven	
6.		$8k \times 8$ RAM.	5
***	(b)	$8k\times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC.	
 6. 7. 		$8k \times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC. Draw and explain the working of a 4-bit	
***	(b)	$8k\times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC.	5
***	(b)	$8k \times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC. Draw and explain the working of a 4-bit	
***	(b)	$8k \times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC. Draw and explain the working of a 4-bit SISO shift register with appropriate timing	5
***	(b)	$8k \times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC. Draw and explain the working of a 4-bit SISO shift register with appropriate timing waveform.	5
7.	(b)	$8k \times 8$ RAM. Explain how a CMOS logic IC can be driven by a TTL logic IC. Draw and explain the working of a 4-bit SISO shift register with appropriate timing waveform. Explain the concept and design procedure of	5

Simplify the given Boolean expression using 8. K-map: $F = \sum m(0, 1, 3, 7, 11, 15) + d(2, 4, 6)$ Also implement the simplified expression using NOR gate. 10 9. (a) For a 2-bit number x, design implement $y = 5x^2 + 6x + 1$ using PLA. 5 (b) What do you mean by semiconductor memories? How do you classify them? 5 Obtain Excess-3 and Gray code for the **10.** (a) following: 5 $(1453)_{10}$ (i)

Design and implement a 4-bit binary adder

(ii)

(b)

 $(56)_{10}$

and subtractor.

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