# B.Tech. - VIEP - COMPUTER SCIENCE AND ENGINEERING (BTCSVI) 

Term-End Examination

## ロロ4E5

June, 2017

## BICS-022 : COMPUTER ARCHITECTURE

Time : 3 hours
Maximum Marks : 70
Note: Attempt any seven questions. All questions carry equal marks.

1. (a) Suppose we have two implementations of the same instruction set architecture. Machine A has clock cycle of 1 ns and a CPI of 2.0 for a program and Machine B has a clock cycle of 2 ns and CPI of $1 \cdot 2$ for the same program. Which machine is faster for this program and by how much ? 6
(b) Define the following terms: 4
(i) Linker
(ii) Executable file
(iii) Stored program concept
(iv) Accumulator

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2. What are the possible addressing modes and their possible uses? Explain through examples.
3. Write an assembly language program to evaluate the following arithmetic expression :

$$
\mathrm{A}=\frac{\mathrm{B}+\mathrm{C} * \mathrm{D} \uparrow 2}{\mathrm{E} * \mathrm{~F}}
$$

(a) using a general register computer with two address instructions.
(b) using an accumulator based computer with one address instruction.
(c) using a stack organized computer with zero address instruction.
4. Design an instruction pipeline for a computer. Specify the operations to be performed in each segment. How can the throughput of this pipeline be calculated? 10
5. What are the major hazards that cause the instruction pipeline to deviate from the normal operation? Explain. 10
6. Discuss the following types of dependencies for parallel execution of any program with examples: 10
(a) Data dependencies
(b) Name dependencies
(c) Control dependencies

7. What is the purpose of Tomasulo's approach in a
dynamically scheduled pipeline? Explain.
8. Distinguish between 10
(a) Shared memory and Distributed memory
(b) Coherence and Consistency
9. Distinguish between instruction level parallelism and loop level parallelism. How does a vector processor exploit loop level parallelism? 10
