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**BIELE-015**

# B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00847

## Term-End Examination

## June, 2014

## BIELE-015 : COMPUTER ARCHITECTURE

*Time : 3 hours* *Maximum Marks : 70*

***Note :*** *Attempt **any seven** questions. **All** questions carry **equal** marks. Any missing data may be suitably assumed.*

1. (a) Explain the difference between structure and behaviour in the digital system context. 5

   (b) Give a gate level realization of full adder using AND-OR circuits only. Also write their sum and carry expressions in SOP and POS form. 5

2. (a) List various design aspects in the processor level design. How performance measurement is performed for processor level design ? 5

   (b) With block diagram, explain the function of Micro Programmed Control Unit. 5

3. (a) Write a program to evaluate the arithmetic statement 5

   $$Z := X + Y$$

   with single address instructions (accumulator based CPU) and two address instructions.

(b) What do you understand by addressing modes ? Discuss the various types of addressing modes. 5

4. (a) Explain Booth's algorithm suitable for multiplication of binary numbers represented in 2'S complement form. 5

(b) Perform the multiplication of following using Booth algorithm : 5

$$(-4)*(-5)$$

5. Define the following : 4x2.5

(a) Micro operation

(b) Micro program

(c) Micro instruction

(d) Program Controlled Instructions

6. (a) What do you mean by property of locality of reference ? 5

(b) Explain the concept behind the address translation or address mapping. Give the names of different schemes of address mapping. 5

7. Assume, we have a machine where the CPI (Cycle Per Instructions) is 2.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total is 40% of the instructions. If the miss penalty is 25 clock cycle and the miss rate is 2%, how much faster would the machine be, if all instruction were cache hits ? 10

8. Explain virtual memory organisation and mapping techniques used for it. 10

9. (a) What are the various synchronization problems in system management ? 5

(b) What is interrupt ? Give the different sources of interrupts and explain about them. 5

10. (a) Give the concept of redundancy in association with fault tolerance. 5

(b) Write down the difference between the isolated mapped I/O and the memory mapped I/O. 5