B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00205

Term-End Examination

June, 2014

BIELE-011 : DIGITAL SYSTEM DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. (a) With a neat block diagram of digital computer, explain the concept of the digital systems. *5*

(b) Draw the block diagram of BCD to Seven segment decoder and explain any two of its applications. *5*

2. Design a sequence detector to detect the sequence 0101 using D flip flop for design. *10*

3. (a) Design a counter that counts the decimal digits according to 2,4,2,1 code using T flip flop for design. *5*

(b) What is the difference between serial and parallel transfer ? What type of register is used in each case ? *5*

4. A sequential circuit has four flip flop A, B, C, D and an input x. It is described by the following state equations :

$$A(t + 1) = (CD' + C'D)\,x + (CD + C'D')\,x'$$

$$B(t + 1) = A \qquad C(t + 1) = B \qquad D(t + 1) = C$$

(a) Obtain the sequence of state when x = 1 starting from 0001. *5*

(b) Obtain the sequence of state when x = 0 starting from 0000. *5*

5. (a) Explain the concept of timing and frequency consideration in controller design. *5*

(b) Explain the controller architecture design in detail. *5*

6. (a) Draw a block diagram for PLA control logic and explain its working. *5*

(b) What is the role of ROM and PROM in microprogram control logic ? *5*

7. (a) What is fundamental mode in asynchronous circuits ? Explain in detail with suitable example. *5*

(b) A majority function is generated in a combinational circuit when the output is equal to 1 if the i/p variables have more 1's then 0's. The o/p is 0 otherwise. Design a 3-bit majority function. *5*

8. (a) Write short notes on hazards in combinational and sequential logic circuits. *5*

(b) What is cycle and races in asynchronous circuit ? What are their remedies ? *5*

9. (a) Write the capabilities of VHDL language. *5*

(b) Differentiate data flow and behavioural modelling using an example of full adder. *5*

10. Write VHDL program for BCD to Gray code converter using structural modelling. *10*