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BIEL-025

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00224

Term-End Examination

June, 2014

BIEL-025 : ADVANCED MICRO-PROCESSOR ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. Differentiate between the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessors and multicomputers on the basis of their structures, resource sharing and inter-processor communications. *10*

2. Define the following terms related to parallelism and dependence relations : $4 \times 2\frac{1}{2} = 10$

(a) Computational granularity

(b) I/O dependence

(c) Control dependence

(d) Communication latency

3. Explain the following terms associated with cache and memory architectures : $4 \times 2\frac{1}{2} = 10$

   (a) Low-order memory interleaving

   (b) Physical address cache versus Virtual address cache

   (c) Atomic versus Non atomic memory access

   (d) Memory band width and fault tolerance

4. (a) Compare the instruction set architecture in RISC and CISC processors in terms of instruction formats, addressing modes and cycles per instruction (CPI). 5

   (b) Explain the differences between superscalar and VLIW architecture in terms of hardware and software requirements. 5

5. Consider the following pipeline reservation table : $4 \times 2\frac{1}{2} = 10$

	1	2	3	4
S1	X			X
S2		X		
S3			X	

   (a) What are the forbidden latencies ?

   (b) Draw the state transition diagram.

   (c) List all the simple cycles and greedy cycles.

   (d) Determine the optimal constant latency cycle and the minimal average latency.

6. Briefly describe the following terms associated with multicomputer networks and message-passing mechanism : $4 \times 2\frac{1}{2} = 10$

   (a) Store and forward routing at packet level

   (b) Wormhole routing at flit level

   (c) Buffer deadlock versus Channel deadlock

   (d) Virtual channels versus Physical channels

7. Explain the following memory organisations for vector accesses : $2 \times 5 = 10$

   (a) C – accesses memory organisations

   (b) C/s – accesses memory organisations

8. What is the significance of the following terms associated with compound vector processing : $4 \times 2\frac{1}{2} = 10$

   (a) Systolic program graphs

   (b) Compound vector functions

   (c) Pipeline network or pipenets

   (d) Vector loops and pipeline chaining

9. (a) What are the unique features of the message driven processor (MDP) making it suitable for building fine-grain multicomputer ? 5

   (b) What are the functions of the address arithmetic unit (AAU) ? 5

10. Design a binary integer multiply pipeline with five stages. The first stage is for partial product generation. The last stage is a 36-bit carry-look ahead adder. The middle three stages are made of 16 carry-save adders (CSAs) of appropriate lengths.

Prepare a schematic design of the five-stage multiply pipeline. All line widths and interstage connections must be shown. What is the maximal throughput of this pipeline in terms of 36-bit results generated per second ? *10*
