No. of Printed Pages : 2

BIEL-012

B.Tech. ELECTRONICS AND COMMUNICATION ENGINEERING

(BTECVI)

00714

Term-End Examination

June, 2014

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks.*

1. (a) Illustrate the concept of mixed signal design with the help of an example. *5*

(b) Explain the mixed signal layout issues. *5*

2. Explain a simple sample and hold circuit with the help of a circuit diagram and characteristics graph. *10*

3. For a 3-bit DAC with R-2-R ladder architecture, let R = 1 kΩ, R_F = 2 kΩ and V_{ref} = 5 V. Determine I_{tot} and V_{out} for D = 100 and 101. *10*

4. With the help of a neat diagram, explain cyclic and pipelined DAC. *10*

5. Discuss in detail the structure of Analog multiplier with suitable diagram. *10*

6. Develop an expression for the effective number of bits in terms of measured SNR if the input sine wave has a peak amplitude of 40% of $(V_{ref+} - V_{ref-})$ *10*

7. Describe the accumulate and dump circuit for decimation and averaging with the help of block diagram. *10*

8. What are the delay elements ? Explain how they are realized using pass transistors, inverters and clocked CMOS. *10*

9. Explain small signal bandwidth output swing, linearity, supply rejection and slew rate with reference to an OP-AMP. *10*

10. Write short notes on any ***two*** of the following : *5×2=10*

    (i) DAC specifications

    (ii) Accuracy issues of flash ADC

    (iii) Band Pass Sync filters