## B.Tech. – VIEP – COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

00927

## Term-End Examination June, 2014

## **BICS-022: COMPUTER ARCHITECTURE**

| Tin   | ne : 3 n | ours Maximum Marks   | Maximum Marks: 70 |  |
|---|----------|--|-------------------|--|
| <b>Note:</b> Attempt any <b>seven</b> questions. Each question carries equal marks. |          |  |                   |  |
| 1.  | (a)      | Discuss the difference between tightly coupled and loosely coupled multiprocessors.                              | 5                 |  |
|   | (b)      | Explain about Memory Addressing.   | 5                 |  |
| 2.  | (a)      | Explain how node duplication helps in achieving superior performance in a multiprocessor scheduling environment. | 5                 |  |
|   | (b)      | Discuss various types of pipelining hazards.   | 5                 |  |
| 3.  | (a)      | Define Instruction level Parallelism with an example.  | 5                 |  |
|   | (b)      | Discuss High performance Instruction delivery.   | 5                 |  |
| 4.  |          | t is Virtual Memory? Discuss protection of a ented virtual memory in the Pentium.                                | 10                |  |
|   | segm     | ented virtual memory in the rentium.   | 10                |  |
| RIC   | <u> </u> | 1 P  | T O               |  |

| <b>5.</b> | Explain the four types of communication patterns in Multicomputer Networks.  10 |   |    |  |
|-----------|---|---|----|--|
| 6.        | Explain the computer classification based on the following:                     |   |    |  |
|           | (i)   | SISD  |    |  |
|           | (ii)  | SIMD  |    |  |
|           | (iii)   | MISD  |    |  |
|           | (iv)  | MIMD  |    |  |
| 7.        | in a  | and discuss the pipelined execution of task<br>Superscalar and VLIW processor. Make<br>sary assumptions of your choice. | 10 |  |
| 8.        | (a)   | Explain practical issues in interconnecting networks.   | 5  |  |
|           | (b)   | Explain ways of reducing Cache Miss penalties and Miss rate.  | 5  |  |
| 9.        | Show<br>synch<br>maste  | ronous bus output to a slave from a bus   | 10 |  |
| 10.       | Explain any <b>two</b> of the following: $5\times 2=10$                         |   |    |  |
|           | (a)   | Multithreading  |    |  |
|           | (b)   | RISC and CISC   |    |  |
|           | (c)   | Multicore architecture  |    |  |