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BIELE-015

01040

B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

June, 2013

BIELE-015 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any seven** questions. All questions carry equal marks. Any missing data may be suitably assumed.*

1. (a) Explain what is meant by a hardwired implementation of a control input ? 5

   (b) Explain the function of arithmatic circuit with the help of circuit diagram. 5

2. (a) What is meant by cache mapping ? What are different types of mapping ? Discuss different mapping techniques with examples. 5

   (b) When a DMA module takes control of a bus and while it retains control of the bus, what does the processer do ? 5

3. Explain microprogram sequences with block diagram. Compare horizontal and vertical organisation. 10

4. (a) Show that for an n- level hierarchical memory system the average access time 6

$$T(n) = \sum_{i=1}^{n} [H(s_n) - H(s_{i-1})]\, t_i$$

Where t_i is the access time of i^{th} level.

(b) Give an algorithm for floating point addition. Illustrate it with an example. 4

5. (a) Write short note on pipeline processing. 4

(b) The details of four level hierarchical memory system are summarized as follows : 6

Level	Component type	Access time	hit ratio
1	ECL main memory	$t_1 = 100$ ns	$H(S_1) = 0.6$
2	Core memory	$t_2 = 10$ μs	$H(S_2) = ?$
3	Disk	$t_3 = 0.5$ ms	$H(S_3) = 0.9$
4	Tape	$t_4 = 50$ ms	$H(S_4) = 1$

Determine $H(s_2)$ if the average access time of this memory hierarchy is found to be 5.1005 ms.

6. Draw the data-path of the $2^{'s}$ - complement multiplier. Give the Robertson's multiplication algorithm for $2^{'s}$ complement fractions. Also illustrate the algorithm for $2^{'s}$ - complement fraction by a suitable example. 10

7. (a) Using LRU policy, calculate the hit ratio for the s beam of page references 6

2, 3, 2, 4, 6, 2, 5, 6, 1, 4, 6

Assume the main memory has three frames and initially all of them are vacant.

(b) What do you understand by multilevel memories ? Explain using suitable diagrams. 4

8. Construct 512 bytes RAM and 512 bytes ROM using 128×8 RAM and 512×8 ROM. 10

9. (a) Write a short note on RISC based instruction format. 5

(b) Differentiate RISC and SISC based microprocessors. 5

10. Write short notes on ***any two*** of the following : **2x5=10**

(a) Programmed I/O

(b) Interrupt driven I/O

(c) DMA controlled I/O