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BIEL-012

01890

B.Tech. Electronics and Communication Engineering (BTECVI)

Term-End Examination

June, 2013

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *(i) Attempt **any seven** questions.*

(ii) Assume suitable missing data, if any.

1. State and explain ADC specifications. **10**

2. A 8 bit resistor string DAC was fabricated with normal resistor value of 1kΩ. If the process was able to provide matching of resistors within 1%, find the maximum INL and DNL of converter assume $V_{REF} = 5V$. **10**

3. Explain the problems associated with single slope ADC and possible solutions. **10**

4. Draw block diagram of two stage opamp with output buffer. Illustrate the various steps for designing such an opamp. **10**

5. How SNR is improved by averaging ? Aid your answer with suitable example. **10**

6. Show that multiplying quad acts as multiplier when all MOSFETs in the multiplying quad have same threshold voltage. 10

7. Explain the role of decimation filters in ADC. 10

8. Explain how resistors and capacitors are fabricated in submicron technology. Also describe the MOSFET behaviour as switch. 10

9. Discuss floor planning, power supply and grounding issues in mixed signal layouts. 10

10. Write short note on *any two* : 2x5=10

(a) Current steering DAC

(b) Sample and hold characteristics

(c) Level shifting circuits

(d) Delay element