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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

00203

December, 2018

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. (a) Explain the difference between signal and variable in VHDL with examples. 5

(b) Explain the different types of objectives in VHDL. What are the predefined data types that exist in VHDL ? 5

2. (a) Explain design flow for digital system design using VHDL. 5

(b) Write a function in VHDL for 4-bit binary to gray code conversion. 5

3. Write a VHDL code for 4-bit ALU to perform arithmetic operations such as addition, subtraction, increment, decrement and logic operations such as AND, OR, XOR and NOT. *10*

4. (a) Explain the architecture of FPGA. Write the difference between FPGA and CPLD. *5*

   (b) Write a VHDL code for 3 to 8 decoder using case statement. *5*

5. (a) Explain the advantages of boundary scan description language. *5*

   (b) What are the types of tests a VLSI chip undergoes ? Discuss. *5*

6. (a) Differentiate between design verification and test evaluation. *5*

   (b) Discuss about different levels of fault models. *5*

7. (a) Explain the simulation steps of design verification with suitable diagram. *5*

   (b) What is the difference between controllability and observability ? *5*

8. (a) What is BIST ? How is a mutual comparator useful for memory BIST ? Explain with suitable block diagram. *5*

   (b) Explain the ad-hoc design for testability techniques. *5*

9. (a) What is the difference between simulation and synthesis ? Explain with suitable example. *3*

(b) What are the fault types and fault models that exist is VLSI testing ? Explain with suitable diagram. *5*

(c) Explain the problems associated with simulation-based design verification. *2*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Test Pattern Generation

(b) Subprograms and Overloading

(c) Design for Testability