B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00293

Term-End Examination

December, 2016

BIELE-015: COMPUTER ARCHITECTURE

Tir	ne : 3	hours Maximum Mari	Maximum Marks: 70	
Note:		Attempt any seven questions. All questions carry equal marks. Any missing data may be suitably assumed and mentioned.		
1.	(a)	Explain the concept of Virtual memory.	5	
	(b)	Draw the block diagram of a 4-bit binar incrementer.	y 5	
2.	(a)	Differentiate between hard-wired an micro-programmed control unit.	d 5	
	(b)	Explain Auto increment/decrement mode of addressing.	of 5	
3.		lain the importance of Associative memorits operation.	y 10	
4.	(a)	Define and explain the working of multipl interrupts.	e 5	
	(b)	Explain about RISC architecture.	5	
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Explain the following data transfer schemes with			
neat diagrams:			
(a)	Interrupt driven data transfer		
(b)	DMA data transfer		
(a)	What do you understand by indexed addressing mode?	5	
(b)	What are the various functions of I/O module?	5	
(a)	List out the methods used to improve the system performance.	5	
(b)	Explain the architecture of a basic computer.	5	
(a)	Describe the techniques for handling control hazard in pipelining.	5	
(b)	Explain the dynamic branch prediction technique.	5	
		10	
	·	· =10	
(a)	DMA Controller		
(b)	Peripheral Component Interface Bus		
(c)	Non-Restoring Division Technique		
	neat (a) (b) (a) (b) (a) (b) Discurrent (a) Write follow (a) (b)	 (a) Interrupt driven data transfer (b) DMA data transfer (a) What do you understand by indexed addressing mode? (b) What are the various functions of I/O module? (a) List out the methods used to improve the system performance. (b) Explain the architecture of a basic computer. (a) Describe the techniques for handling control hazard in pipelining. (b) Explain the dynamic branch prediction technique. Discuss shared memory multiprocessor with a neat diagram. Also define multithreading. Write short notes on any two of the following: 2×5 (a) DMA Controller (b) Peripheral Component Interface Bus 	