

**MCA (Revised) / BCA (Revised)**

**Term-End Examination**

05286

**December, 2016**

**MCS-012 : COMPUTER ORGANISATION AND  
ASSEMBLY LANGUAGE PROGRAMMING**

*Time : 3 hours*

*Maximum Marks : 100*

*(Weightage 75%)*

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**Note :** Question number 1 is **compulsory** and carries 40 marks. Attempt any **three** questions from the rest.

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1. (a) State *True* or *False* with a brief justification (if false). 5
- (i) Boolean relation  $A + AB = B$ .
  - (ii) Hardware interrupts can be invoked with the help of INT function.
  - (iii) 8086 has a 16-bit data bus and a 20-bit address bus.
  - (iv) Wilkes Control does not provide a branching microinstruction.
  - (v) 1 MB equals  $2^{30}$  bits.

- (b) Represent the number 1110·0011 in IEEE 754 floating point single precision number representation. 6
- (c) Perform the following arithmetic operations : 6
- (i) Add (-125) and (-105) in 8-bit register using signed 2's complement representation of negative numbers. Also indicate overflow, if any.
- (ii) Convert the decimal number 789 to octal, hexadecimal and BCD.
- (d) Simplify the following expression using Karnaugh map in sum of the products form :  

$$F(A, B, C, D) = \Sigma(1, 3, 5, 7, 9, 11, 13, 15)$$
 Also draw the logic circuit for the simplified expression. 5
- (e) Design a 4-bit serial input shift register and explain its working. 5
- (f) Draw a suitable diagram and explain the execution of subroutines CALL & RETURN using stack. 5

- (g) An 8-bit register contains the binary value 11001101. What is the register value after an arithmetic shift right ? State whether there is an overflow. 3
- (h) Write a program in 8086 assembly language that counts the number of characters in a string stored in the data segment. 5
2. (a) What is Von-Neumann architecture ? Explain. 4
- (b) Draw an internal organization of  $32 \times 4$  RAM and explain the purpose of control signals used here. 5
- (c) Demonstrate the use of Hamming code for a 4-bit word sequence transmitted as 1000 whereas received as 1100. Make suitable assumptions. 5
- (d) With reference to the instruction execution, explain how the following steps are performed and by which component : 6
- (i) Calculate the address of the next instruction to be executed.
- (ii) Decode the instruction.
- (iii) Computation of operand's address.

3. (a) How can interleaved memory mechanism be used to improve the overall processing speed of a computer system ? Explain with the help of a diagram. 5
- (b) How many RAM chips of size  $512\text{ K} \times 1\text{ bit}$  are required to build  $1\text{ M}$  byte main memory ? 3
- (c) A digital computer has a memory unit of  $64\text{ K} \times 16$  and a cache memory of  $1\text{ K}$  words. The cache uses direct mapping with a block size of four words. How many bits are there in tag, index and block fields of the address ? 6
- (d) Define the following terms : 6
- (i) Seek time
  - (ii) Latency time
  - (iii) Hit ratio in cache
4. (a) Draw a logic diagram of one stage of logic circuit for implementation of AND, OR, XOR and complement microoperations. Also draw and explain its functional representation. 6

- (b) Differentiate between the following : 6
- (i) Hardwired v/s Microprogrammed control
  - (ii) Horizontal v/s Vertical microinstructions
- (c) What is the purpose of multiple segments in 8086 ? 4
- (d) Explain the following 8086 microprocessor addressing modes with the help of an example for each : 4
- (i) Register Indirect
  - (ii) Based Indexed
5. (a) Write a step-by-step process to explain how an interrupt is handled by a computer. 6
- (b) Draw the logic diagram of JK flip-flop along with its characteristic table and excitation table. Explain various state transitions. 8
- (c) Write an assembly program using 8086 assembly language that adds two 2-digit packed BCD numbers stored in the memory. Make suitable assumptions. 6