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BIELE-015

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2015

BIELE-015 : COMPUTER ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any **seven** questions. All questions carry equal marks. Any missing data may be suitably assumed and mentioned.*

1. (a) Discuss Fixed Point and Floating Point number representation with suitable examples. *5*

(b) How is performance measurement performed for processor level design ? *5*

2. (a) Show the data flow in different registers used in shift and add multiplication hardware for multiplying + 13 and – 12. *5*

(b) What types of instructions should be included in a general purpose processor's instruction set ? Categorise them. *5*

3. (a) What is CISC ? Explain its characteristics. 5

(b) With a suitable diagram, explain the addition of two floating point numbers with the help of pipeline process. 5

4. Draw a space-time diagram for a six-segment pipelining showing the time it takes to process eight tasks. A non-pipeline system takes 50 ns to process a task. The same task can be produced in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed-up ratio of the pipeline for 100 tasks. What is the maximum speed-up that can be achieved ? 10

5. (a) Explain the function of cache memory. How is it implemented ? 5

(b) How can virtual memory offer more memory than is really present in the primary memory to the software developer ? 5

6. (a) What do you mean by 'locality of reference' ? How many 128 × 8 RAM chips are needed to provide a memory capacity of 1024 bytes ? 5

(b) Explain the concept behind the address translation or address mapping. 5

7. (a) A direct mapped cache has the following parameters :

Cache size = 1 K words

Block size = 128 words

Main memory size = 64 K words

Specify the number of bits in TAG, BLOCK and WORD in main memory. *5*

(b) What are the various modes of data transfer between CPU and I/O devices ? *5*

8. (a) What is the need of I/O controller ? *5*

(b) Explain bus arbitration using Polling works with necessary diagram. What is the advantage of Polling works over Daisy chaining ? *5*

9. With a neat block diagram, explain how DMA controller is initiated for DMA data transfer. *10*

10. Write short notes on any ***two*** of the following : *2×5=10*

(a) Pipeline Processing

(b) Associative Memory

(c) Isolated versus Memory Mapped I/O