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BIELE-003

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2015

BIELE-003 : MODELLING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. All questions carry equal marks. Missing data, if any, may be suitably assumed and mentioned. Use of scientific calculator is permitted.*

1. Differentiate between Behavioural Modelling and Structural Modelling with the help of an example. *10*

2. (a) Write VHDL code for a full subtractor using logic equations. *5*

(b) Explain signal attributes with an example. *5*

3. (a) Differentiate between inertial delay and transport delay with the help of suitable examples. *5*

(b) Define Generics. Write an entity for an AND gate that has three generics associated with it. *5*

4. What is operator overloading ? Write VHDL package with overload operators for bit vectors. *10*

5. (a) What is subprogram ? Explain it with a suitable example. *5*

   (b) What is fault dominance ? Explain it with a suitable example. *5*

6. Discuss different types of faults found in digital circuits. *10*

7. (a) Why is testing required for digital circuits ? What is meant by observability and controllability of the circuit ? *5*

   (b) Explain single and multiple stuck faults, with suitable examples. *5*

8. Explain Ad-hoc design for testability techniques with suitable diagrams. *10*

9. (a) Draw and explain typical BIST hardware. *5*

   (b) Explain Pseudo-exhaustive testing and Pseudo-random testing. *5*

10. Write short notes on any ***two*** of the following : *2×5=10*

    (a) Data Objects and Types

    (b) FPGA Architectures and Design

    (c) Classical Scan Design
