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**BIEL-025**

# B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

## Term-End Examination

## December, 2015

## BIEL-025 : ADVANCED MICROPROCESSOR ARCHITECTURE

*Time : 3 hours* *Maximum Marks : 70*

***Note :*** *Attempt any **seven** questions. All questions carry equal marks. Use of scientific calculator is allowed.*

**1.** Characterise the architectural operations of SIMD and MIMD computers. Distinguish between multiprocessor and multicomputer on the basis of their structures, resource sharing and interprocessor communications. *10*

**2.** Compare the instruction-set architecture in RISC and CISC processors in terms of instruction formats, addressing modes and cycles per instructions (CPI). Also mention the difference between superscalar and VLIW architectures in terms of hardware and software requirements.

*6+4=10*

3. Explain the following terms associated with memory management : *2×5=10*

   (a) The role of a memory manager in an operating system (OS) kernel

   (b) Demand paging memory system and Swapping memory system, with examples

4. Consider a cache ($M_1$) and memory ($M_2$) hierarchy with the following characteristics :

   $M_1$ : 16 K words, 50 ns access time

   $M_2$ : 1 M words, 400 ns access time

   Assume eight-word cache blocks and a set-size of 256 words with set-associative mapping.

   (a) Show the mapping between $M_2$ and $M_1$.

   (b) Calculate the effective memory-access time with a cache hit ratio of h = 0·95. *5+5=10*

5. The hardware cost of a new m-stage, single function pipeline is approximated by 22 m + 30. The latency of the function to be executed is 90 ns, if pipelining is not used. The pipelined implementation's interstage buffers are expected to add an additional 10 m ns to this latency. Estimate the number of stages needed to optimize the pipeline's performance/cost ratio. *10*

6. Define the following terms related to modern processor technology : *5×2=10*

(a) Processor design space

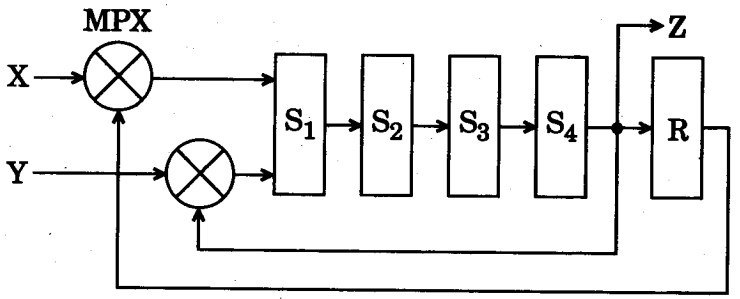
(b) Resource conflicts

(c) Hardwired versus Micro-coded control

(d) Unified versus Split caches

(e) Instruction issue rate

7. Consider an adder pipeline with four stages as shown below. The pipeline consists of input lines X and Y, output line Z and a register R.




(a) Assume that the elements of the vector A are fed into the pipeline through input X, one element per cycle. What is the minimum number of clock cycles required to compute the sum of an N-element vector

$$A : s = \sum_{I=1}^{N} A(I) ?$$

Neglect the set-up time for the pipeline and consider 'O' as input into the pipeline by default in the absence of an operand.

(b) Find $N_{1/2}$, the minimum vector length required to achieve half of the maximum speed-up. *5+5=10*

**8.** Design a 16-bit priority encoder using two copies of an 8-bit priority encoder. Use additional gates of any standard type while designing, if required. *10*

**9.** Instructions such as 'store' instruction that modify memory make it difficult to support precise interrupts in pipelined CPUs. Why is this so ? Outline a design method to solve this problem. *10*

**10.** Consider the five-stage pipelined processor specified by the following reservation table :

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| $S_1$ | × | | | | | × |
| $S_2$ | | × | | | × | |
| $S_3$ | | | × | | | |
| $S_4$ | | | | × | | |
| $S_5$ | | × | | | | × |

(a) List the set of forbidden latencies and the collision vector.

(b) Draw a state transition diagram showing all possible initial sequences without causing a collision in the pipeline.

(c) Identify the greedy cycles among the simple cycle.

(d) What will be the maximum throughput of this pipeline ? $4 \times 2\frac{1}{2} = 10$