No. of Printed Pages : 4

BIEL-025

B.Tech. – VIEP – ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

00530

Term-End Examination

December, 2014

BIEL-025 : ADVANCED MICROPROCESSOR ARCHITECTURE

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt any* ***seven*** *questions. All questions carry equal marks.*

1. Indicate whether each of the following statements are *true* or *false* and justify your answer with reasoning and supportive examples.

(a) The CPU computations and I/O operations cannot be overlapped in a multiprogrammed computer. *5*

(b) Synchronization of all PEs in an SIMD computer is done by hardware rather than by software as is often done in most MIMD computers. *5*

2. Define the following terms related to parallelism and dependence relations : $4 \times 2\frac{1}{2} = 10$

   (a) Degree of parallelism
   (b) Anti dependence
   (c) Resource dependence
   (d) Bernstein's conditions

3. Explain the significance of the following terms associated with cache design : $4 \times 2\frac{1}{2} = 10$

   (a) Write-through versus Write-back caches
   (b) Cache flushing policies
   (c) Factors affecting cache hit ratio
   (d) Cacheable versus Non cacheable data

4. (a) Explain the 'inclusion property' and 'memory coherence' requirements in a multilevel memory hierarchy. 5

   (b) Distinguish between write-through and write-back policies in maintaining the coherence in adjacent levels. 5

5. Explain the following terms associated with multicomputer networks and message-passing mechanism : $4 \times 2\frac{1}{2} = 10$

   (a) Message, packets and flits
   (b) Buffering flow control using virtual cut-through routing
   (c) Discard and retransmission flow control
   (d) Blocking flow control in wormhole routing

6. Distinguish among the following vector processing machines in terms of architecture, performance range, and cost-effectiveness : $2 \times 5 = 10$

(a) High-end mainframes or near-supercomputers

(b) Mini supercomputers or super computing workstations.

7. Consider the five-stage pipelined processor specified by the following reservation table : $4 \times 2\frac{1}{2} = 10$

	1	2	3	4	5	6
S1	X					X
S2		X			X	
S3			X			
S4				X		
S5		X				X

(a) List the set of forbidden latencies and the collision vector.

(b) List all the simple cycles from the state diagram.

(c) Identify the greedy cycles among the simple cycle.

(d) What will be the maximum throughput of this pipeline ?

8. (a) Why has shared virtual memory (SVM) become a necessity in building a scalable system with memories physically distributed over a large number of processing nodes ? 5

(b) What are the major differences in implementing SVM at the cache block level and page level ? 5

9. Define the following loop transformations and discuss how they can be applied for loop vectorization or parallelization : $4 \times 2\frac{1}{2} = 10$

(a) Loop permutation

(b) Loop skewing

(c) Wavefront transformation

(d) Software pipelining

10. A computer system has a 128-byte cache. It uses four-way set associative mapping with 8 bytes in each block. The physical address size is 32 bits, and the smallest addressable unit is 1 byte.

(a) Draw a diagram showing the organization of the cache and indicating how physical address is related to cache address. 5

(b) To what block frames of the cache can the address $(000010AF)_{16}$ be assigned ? 5