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BIEL-012

B.Tech. Electronics and Communication Engineering (BTECVI)

Term-End Examination

December, 2013

BIEL-012 : ANALOG AND MIXED MODE VLSI DESIGN

Time : 3 hours *Maximum Marks : 70*

*Note : (i) Attempt **any seven** questions.*

*(ii) All questions carry **equal** marks.*

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1. (a) State the reasons for pedestal error, droop aperture error and sampling error. **5**

(b) Explain ADC specifications. **5**

2. (a) Define resolution, DNL, INL and VFS with respect to DAC. **5**

(b) Explain the concept of aliasing. **5**

3. An 8 bit single slope ADC with $V_{ref} = 5V$ is used to convert a slow moving analog signal. What is the maximum conversion time with $f_{clk} = 1$ MHz ? What is the maximum frequency of analog signal ? **10**

4. Explain qualitatively the architecture and working of a charge scaling DAC. **10**

5. Discuss basic CMOS comparator design with the help of suitable diagram. **10**

6. Draw the circuit arrangement used for decimation and averaging and explain the same. Also determine the transfer function for the same. **10**

7. Provide general interpolation topology. Draw and explain the block diagram of a DAC with interpolator. **10**

8. (a) Describe the submicron CMOS process flow. **5**

   (b) Explain how MOSFET behaves as a capacitor and explain floating MOS capacitor also in brief. **5**

9. With respect to the block diagram of a generic OP-AMP, evolve and explain an OP-AMP design. **10**

10. Write a short note on ***any two*** of the following : **5x2=10**

    (a) Mixed signal layout issues.

    (b) 2 - step flash ADC.

    (c) Multiplying Quad.
