No. of Printed Pages : 2

BIELE-003

01053

B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2012

BIELE-003 : MODELING AND TESTING OF DIGITAL SYSTEMS

Time : 3 hours *Maximum Marks : 70*

Note : *(1) Attempt any **seven** questions.*
(2) Assum suitable missing data if any.

1. (a) What is the significance of CAD tools ? Provide design flow for digital circuit design. 5

   (b) Provide basic terminology of VHDL and explain features of VHDL. 5

2. Explain different types of hardware abstraction levels of a digital design. 10

3. Explain Sub programs and over loading in detail. Why these are required ? 10

4. Draw general FPGA architecture and explain complete design flow using FPGA in detail. 10

5. (a) Explain process constructs and various signal assignments in VHDL. 4

(b) Assume that four bit serial load shift register contains an input stuck-at-o fault at its second and third bits owing to manufacturing imperfection. Design an input test sequence to demonstrate these failures at the o/p's of this shift register. 6

6. Explain fault models and fault equivalency. 10

7. Analyze the equivalency of stuck at faults in a full adder and identify the minimum number of tests detecting all testable faults. 10

8. Discuss design for testability and explain adhoc design for testability techniques. 10

9. Explain Built in Self Test (BIST) architecture in detail with suitable examples. 10

10. Write short note on **any two** : 5x2=10

(a) Delay modelling.

(b) Package and Libraries.

(c) VHDL basic language elements.
