00801

B.TECH. - ELECTRICAL ENGINEERING

Term-End Examination

December, 2012

BIEE-017 : DIGITAL ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any seven** questions from question no **1** to **10**.*

1. (a) Explain the working of full - Adder. Draw its truth table. 8

(b) Execute the following program according to Intel 8085 instructions. 2

```
L×1     H, 2000 H
MOV     B, M
        HLT
```

2. Describe the Architecture of Intel 8086 Microprocessor. 10

3. Describe the registers of Intel 8085 Microprocessor. 10

4. (a) Write an assembly language program starting from memory location 2400 H to subtract digital number 48 stored in memory location 2421 H from decimal number 99 stored in memory location 2420 H. The answer should be in decimal numbers and stored in memory location 2422 H. **4**

(b) Explain REP Prefix and Segment Override Prefix. **6**

5. Explain the following assembler directives **10**

(a) DB (b) DW (c) DD

(d) EQU (e) END

6. What is an Interrupt ? Differentiate between Vectored interrupt and the nonvectored interrupt. Draw a possible vectored interrupt configuration. **10**

7. (a) Explain 4-bit synchronous binary counter. **5**

(b) Explain 4 bit up - down binary counter. **5**

8. (a) How many flip-flops must be complemented in a 10-bit binary ripple - counter to reach the next count after 0111111111 ? **3**

(b) Construct a Johnson - counter with ten timing signals. **7**

9. (a) Explain the 4-bit Bidirectional Shift Register with Parallel Load. Write it's function table also. 5

(b) Draw the logic diagram (showing all gates) of a master - slave D flip - flop. Use NAND gates. 5

10. (a) Design a sequential circuit with JK flip flops to satisfy the following state equations : 5

$A\ (t+1) = A'B'CD + A'B'C + ACD + AC'D'$

$B\ (t+1) = A'C + CD' + A'BC'$

$C\ (t+1) = B$

$D\ (t+1) + D'$

(b) Design a BCD - to - decimal decoder. 5