No. of Printed Pages : 3

BIEL-003

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B.TECH. IN ELECTRONICS AND COMMUNICATION ENGINEERING (BTECVI)

Term-End Examination

December, 2012

BIEL-003 : DIGITAL ELECTRONICS

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **seven** questions in all. All the questions are to be answered in English-language only.*

1. (a) Simplify the logical expression using Boolean algebra method. 5

$Y = AB + \overline{AC} + A\overline{B}C\,(AB + C)$

(b) Use K-map to reduce the given expression to a minimum sum of products form. 5

$Y = \overline{A}B\,(\overline{C}\,\overline{D} + \overline{C}\,D) + AB(\overline{C}\,\overline{D} + \overline{C}D) + A\overline{B}\overline{C}D$

2. (a) Substract using r's complement $(60)_{10} - (41.75)_{10}$ 5

(b) Find the value of base $-x$. $(211)_x = (152)_8$ 5

3. (a) Design a full adder circuit using gates. 5

(b) Find the canonical form for the following functions : 5

(i) $F(A,B,C) = \Sigma m(0, 1, 4, 7)$

(ii) $F(A,B,C) = AB + BC$.

4. (a) Design a 3 bit Binary to Gray code converter. 5

(b) Input A,B,C,D are available. Using 8 : 1 MUX implement the function. 5

$F(A, B, C, D) = \Sigma m (0, 2, 4, 5, 7, 9, 11)$

5. (a) Draw the logic diagram of master-slave J-K flip-flop using NAND gates only. 5

(b) Design a synchronous counter with the following repeated binary sequence 0, 1, 3, 5, 7, 9, 11, 13, 15. Use J-K flip-flop. 5

6. (a) Draw the logic diagram of S – P flip-flop and write the excitation table. 5

(b) Draw the logic diagram of J-K flip-flop and write the characteristic table. 5

7. (a) Write a brief note on interfacing TTL with CMOS. 5

(b) Compare the characteristics of different logic families. 5

8. (a) What is meant by multiple-emitter transistor ? Explain in brief. 5

(b) What happens if any input of TTL circuit is kept floating ? 5

9. (a) Design a BCD to seven segment decoder using PROM. 5

(b) Design a BCD to seven segment decoder using PLA. 5

10. (a) Write a short note on RAM. 5

(b) Write a short note on PROM. 5