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BICS-009

00681

B.TECH. IN COMPUTER SCIENCE AND ENGINEERING (BTCSVI)

Term-End Examination

December, 2012

BICS-009 : LOGIC DESIGN

Time : 3 hours *Maximum Marks : 70*

Note : *Attempt **any seven** questions. All questions carry **equal** marks. All questions are in English. Answers should be in English.*

1. (a) Implement the following boolean function using NOR gates only : 5

$$F = \left(A\,\overline{B} + \overline{A}\,B\right)\left(C + \overline{D}\right)$$

(b) "Static - O Hazard" - Explain this in brief. 5

2. (a) Simplify the boolean function using Quine MC Clusky method : 6

$f(x_1,x_2,x_3,x_4) = \Sigma m(0,5,7,8,9,10,11,14,15)$

(b) Show how using a 3 − to −8 decoder and multi input OR gates following Boolean expressions can be realized simultaneously : 4

F_1 (A, B, C) $= \Sigma m$ (0, 4, 6)

F_2 (A, B, C) $= \Sigma m$ (0, 5)

F_3 (A, B, C) $= \Sigma m$ (1, 2, 3, 7)

3. (a) Using 4 I/P multiplexer implement the following function : 5

F (A, B, C) = Σm(0, 2, 3, 5, 7) Use B, C as select inputs.

(b) Design a octal to binary encoder. 5

4. (a) Add +39 and −22 in 2's complement method. 4

(b) Design a 4 bit binary adder subtractor combinational circuit. 6

5. (a) Explain a schmitt trigger transfer characteristic. 5

(b) Show how a D flip-flop can be converted to SR flip-flop ? 5

6. (a) Explain the operation of JK master slave flip-flop. 6

(b) Explain switched tail counter operation in brief. 4

7. (a) Design a MOD − 6 synchronous counter using JK-flip-flop. 6

(b) Explain 3 bit binary ripple counter. 4

8. (a) Explain Mealy and Moore models of synchronous sequential circuit. 5

(b) An a synchronous sequential circuit is described by excitation function : 5

$Y = x_1 \bar{x}_2 + x_1 y$ and O/P function $Z = x_1 x_2 y$

(i) Draw the logic diagram of a circuit

(ii) Derive the transition table and O/P map.

9. Write short notes on ***any two*** : **10**

(a) Binary ladders

(b) Continuous A/D conversion

(c) Successive approximation A DC

10. Write short notes on ***any two*** : **10**

(a) Open collector TTL NAND gate

(b) 74 COO CMOS NOR gate

(c) Noise Immunity